AMENDMENTS TO THE CLAIMS

Following is a listing of all claims in the present application, which listing supersedes all previously presented claims:

Listing of the Claims

1-19. (Canceled).

20. (Previously Presented) A MOS transistor, comprising:

a T-shaped gate electrode disposed on a semiconductor substrate, the T-shaped gate electrode having a wide portion and a narrow portion, the narrow portion disposed between the wide portion and the semiconductor substrate, so as to have an undercut region adjacent to the narrow portion;

an L-shaped lower spacer covering a top surface of the semiconductor substrate at both sides of the T-shaped gate electrode and covering sides of the wide portion of the T-shaped gate electrode, the L-shaped lower spacer having a first element disposed substantially perpendicular to the semiconductor substrate, and having a second element disposed substantially parallel to the semiconductor substrate, the second element extending from the first element laterally away from the T-shaped gate electrode, wherein the first element and the second element intersect to define a substantially 90 degree angle in an outer surface of the L-shaped lower spacer;

a low-concentration impurity region formed in the semiconductor substrate at both sides of the T-shaped gate electrode;

a high-concentration impurity region formed in the semiconductor substrate next to the L-shaped lower spacer; and

a mid-concentration impurity region disposed between the high- and low-concentration impurity regions.

21. (Previously Presented) The MOS transistor as claimed in claim 20, wherein the T-shaped gate electrode comprises:

lower and upper conductive layer patterns that are sequentially stacked, wherein the upper conductive layer pattern is wider than the lower conductive layer pattern.

22. (Previously Presented) The MOS transistor as claimed in claim 20, wherein the L-shaped lower spacer further comprises a third element extending into the undercut region, the third element disposed substantially parallel to the semiconductor substrate and extending from the first element laterally towards the T-shaped gate electrode.

23. (Original) The MOS transistor as claimed in claim 21, wherein the lower and upper conductive layer patterns are made of materials having an etch selectivity with respect to each other.

24. (Original) The MOS transistor as claimed in claim 21, wherein the lower conductive layer pattern is made of silicon germanium or nitride titanium.

25. (Original) The MOS transistor as claimed in claim 21, wherein the upper conductive layer pattern is made of polysilicon or tungsten.

26. (Previously Presented) A MOS transistor, comprising:

a T-shaped gate electrode disposed on a semiconductor substrate, the T-shaped gate electrode having a wide portion and a narrow portion, the narrow portion disposed between the wide portion and the semiconductor substrate, so as to have an undercut region adjacent

to the narrow portion;

an L-shaped lower spacer covering a top surface of the semiconductor substrate at both sides of the T-shaped gate electrode and covering sides of the wide portion of the T-shaped gate electrode, the L-shaped lower spacer having a first element disposed substantially perpendicular to the semiconductor substrate, and having a second element disposed substantially parallel to the semiconductor substrate, the second element extending from the first element laterally away from the T-shaped gate electrode, wherein the first element and the second element intersect to define a substantially 90 degree angle in an outer surface of the L-shaped lower spacer;

a low-concentration impurity region formed in the semiconductor substrate at both sides of the T-shaped gate electrode;

a high-concentration impurity region formed in the semiconductor substrate next to the L-shaped lower spacer;

a mid-concentration impurity region disposed between the high- and low-concentration impurity regions, and

a surface insulating layer intervened between the narrow portion of the gate electrode and the lower spacer.

27. (Previously Presented) The MOS transistor as claimed in claim 20, wherein the first element of the L-shaped lower spacer completely covers sides of the wide portion of the T-shaped gate electrode.

28. (Previously Presented) The MOS transistor as claimed in claim 20, wherein the second element of the L-shaped lower spacer partially covers the narrow portion of the T-shaped gate electrode.

29. (Previously Presented) The MOS transistor as claimed in claim 20, wherein thicknesses of the first and second elements are approximately the same.

30. (Previously Presented) The MOS transistor as claimed in claim 26, wherein the surface insulating layer completely fills the undercut region.

31. (Previously Presented) The MOS transistor as claimed in claim 26, wherein the surface insulating layer partially, but not completely, fills the undercut region and the L-shaped lower spacer completely fills the remainder of the undercut region.

32. (New) The MOS transistor as claimed in claim 20, wherein a width of the first element, which is measured beside the T-shaped gate electrode, is substantially equal to a thickness of the second element, which is measured on the mid-concentration impurity region.

33. (New) The MOS transistor as claimed in claim 26, wherein a width of the first element, which is measured beside the T-shaped gate electrode, is substantially equal to a thickness of the second element, which is measured on the mid-concentration impurity region.